



September 12, 2003

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
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Subject: | Serial No. 10/600,393 06/20/03 |
| Chi-Chun Chen et al.
| METHOD OF FORMING DUAL GATE
| INSULATOR LAYERS FOR CMOS
| APPLICATIONS
Grp. Art Unit:

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
deposited with the United States Postal Service as first class
mail in an envelope addressed to: Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450, on September 19, 2003.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

 9/19/03

U.S. Patent 6,110,842 to Okuno et al., "Method of Forming Multiple Gate Oxide Thicknesses Using High Density Plasma Nitridation," discloses a process for multiple gate oxides thicknesses using plasma nitridation.

U.S. Patent 6,030,862 to Kepler, "Dual Gate Oxide Formation with Minimal Channel Dopant Diffusion," discloses a DGO process.

U.S. Patent 5,960,289 to Tsui et al., "Method for Making a Dual-Thickness Gate Oxide Layer Using a Nitride/Oxide Composite Region," reveals a DGO using a N/O composition.

U.S. Patent 6,262,455 to Lutze et al., "Method of Forming Dual Gate Oxide Layers of Varying Thickness on a Single Substrate," discloses a DGO process.

U.S. Patent 6,037,224 to Buller et al., "Method for Growing Dual Oxide Thickness Using Nitrided Oxides for Oxidation Suppression," discloses a DGO using nitrided oxides.

Sincerely,



Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION
IN AN APPLICATION

(Use several sheets if necessary)



Document Number (Optional)

TSMC-02-066 10/600,393

Applicant

Chi-Chun Chen et al.

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06/20/03

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